PRACE PATC Course: Intel MIC Programming Workshop

LRZ, 27.6.- 29.6.2016
Information

- Course site:
  LRZ, Boltzmannstr. 1, 85748 Garching b. München, Seminarraum I & Hörsaal

- Tutorials:
  Mon+Tue, interleaved with KNC lectures

- Course material by LRZ, RRZE and Intel

- Workshop Webpage:
  http://www.lrz.de/services/compute/courses/x_lecturenotes/mic_workshop/
  http://goo.gl/xxRNWP

- WIFI: eduroam (https://www.lrz.de/services/netz/mobil/eduroam/)

- Interest in guided SuperMUC tour?
LRZ in the HPC Environment

Leibniz Supercomputing Centre of the Bavarian Academy of Sciences and Humanities

Bavarian Contribution to National Infrastructure

GCS Gauss Centre for Supercomputing

HLRS@Stuttgart  JSC@Jülich  LRZ@Garching

German Contribution to European Infrastructure

PRACE Partnership for Advanced Computing in Europe

PRACE has 25 members, representing European Union Member States and Associated Countries.
Advanced Training Centre (PATC) Courses

LRZ is part of the Gauss Centre for Supercomputing (GCS), which is one of the six PRACE Advanced Training Centres (PATCs) that started in 2012:

- Barcelona Supercomputing Center (Spain), CINECA
- Consorzio Interuniversitario (Italy)
- CSC – IT Center for Science Ltd (Finland)
- EPCC at the University of Edinburgh (UK)
- Gauss Centre for Supercomputing (Germany)
- Maison de la Simulation (France)

**Mission:** Serve as European hubs and key drivers of advanced high-quality training for researchers working in the computational sciences.

http://www.training.prace-ri.eu/
Each PATC is responsible for the implementation of a programme of events aimed to meet the training needs of the research community and to foster HPC skills in general.

- **Advanced Fortran Topics**
  2 days, 2 LRZ lecturers

- **Node-Level Performance Engineering**
  2 days, 2 RRZE lecturers

- **Introduction to hybrid programming in HPC**
  1-day, 1 HLRS & 1 RRZE lecturers

- **Advanced Topics in High Performance Computing**
  4-days, 3 LRZ + 2 RRZE lecturers

- **VI-HPS Tuning Workshop**
  5-days, 15 lecturers, organised by JSC & LRZ

- **Intel MIC Programming Workshop**
  3-days, 3 LRZ + 1 RRZE + 1 Intel lecturers + 4 invited speakers
Intel Xeon Phi and GPU Training

28.-30.4.2014 @ LRZ (PATC): KNC+GPU
27.-29.4.2015 @ LRZ (PATC): KNC+GPU
3.-4.2.2016 @ IT4Innovations: KNC
27.-29.6.2016 @ LRZ (PATC): KNC+KNL
Sept. 2016 @ PRACE Seasonal School, Hagenberg: KNC
Feb. 2017 @ IT4Innovations (PATC): KNC
Jun. 2017 @ LRZ (PATC): KNL

http://inside.hlrs.de/
inSiDE, Vol. 12, No. 2, p. 102, 2014
Acknowledgements

- **RRZE** (Regional Computing Centre of the University Erlangen-Nuremberg).
- Gauss Centre for Supercomputing (**GCS**)
- **IT4Innovation**, Ostrava.
- Partnership for Advanced Computing in Europe (**PRACE**)
- Intel
- **BMBF** (Federal Ministry of Education and Research)
Czech-Bavarian Competence Team for Supercomputing Applications (CzeBaCCA)

New BMBF funded project that started in Jan. 2016 to:

- Foster Czech-German Collaboration in Simulation Supercomputing
  - series of workshops will initiate and deepen collaboration between Czech and German computational scientists
- Establish Well-Trained Supercomputing Communities
  - joint training program will extend and improve trainings on both sides
- Improve Simulation Software
  - establish and disseminate role models and best practices of simulation software in supercomputing
CzeBaCCA Trainings and Workshops

- https://www.lrz.de/forschung/projekte/forschung-hpc/CzeBaCCA/
  - Intel MIC Programming Workshop,
    3 – 4 February 2016, Ostrava, Czech Republic
  - Scientific Workshop: SeisMIC - Seismic Simulation on Current and Future Supercomputers,
    5 February 2016, Ostrava, Czech Republic
  - Intel MIC Programming Workshop,
    27 - 29 June 2016, Garching, Germany
  - Scientific Workshop: High Performance Computing for Water Related Hazards,
    29 June - 1 July 2016, Garching, Germany

http://inside.hlrs.de/

27-29 June 2016
Presenters

● Lecturers:
  – Dr. Momme Allalen, LRZ
  – Dr. Fabio Baruffa, LRZ
  – Dr.-Ing. Jan Eitzinger, RRZE
  – Andrey Semin, Intel
  – Dr. Volker Weinberg, LRZ

● Invited Speakers for Plenum Session
  – Michael Bader, IPCC@TUM
  – Dr.-Ing. Jan Eitzinger, RRZE
  – Luigi Iapichino / Fabio Baruffa, IPCC@LRZ
  – Serhiy Mochalskyy, IPP
  – Andrey Semin, Intel
  – Vit Vondrak, IT4Innovations
Agenda Monday

- 09:00-10:00 Introduction (Weinberg)
- 10:00-10:30 Hardware Overview and Native I (Allalen)
- **10:30-11:00 Coffee Break**
- 11:00-11:30 Hardware Overview and Native II (Allalen)
- 11:30-12:00 Lab: Native Mode
- **12:00-13:00 Lunch Break**
- 13:00-14:00 Offloading Part I (Weinberg)
- 14:00-15:00 Lab: Offloading I
- **15:00-15:30 Coffee Break**
- 15:30-16:15 Offloading Part II (Weinberg)
- 16:15-17:00 Lab: Offloading II
Agenda Tuesday

- 09:00-09:30 MPI (Weinberg)
- 09:30-10:30 Lab: MPI
- **10:30-11:00 Coffee Break**
- 11:00-11:30 MKL (Allalen)
- 11:30-12:00 Lab: MKL I
- **12:00-13:00 Lunch break**
- 13:00-13:30 Lab: MKL II
- 13:30-14:00 Vectorisation & Performance (Allalen)
- 14:00-15:00 Lab: Vectorisation
- **15:00-15:30 Coffee Break**
- 15:30-17:30 Tools for Intel Xeon Phi (Baruffa)
- **18:00 Bus leaving in front of main entrance for social event: Guided tour of Weihenstephan Brewery and dinner**
- **22:00 Bus leaving at Weihenstephan**
Agenda Wednesday Morning

- Wednesday, June 29, 2016, 09:00-12:00, Hörsaal, H.E.009 (Lecture Hall), public session

- 09:00-10:30 Advanced MIC Programming Techniques (SIMD, Intrinsics,... ) (Jan Eitzinger, RRZE)

- 10:30-10:45 Coffee Break

- 10:45-12:00 Knights Landing (KNL) architecture and software (Andrey Semin, Intel)

- 12:00-13:00 Lunch break
Agenda Wednesday Afternoon

- **Wednesday, June 29, 2016, 13:00-18:00, Hörsaal, H.E.009 (Lecture Hall)**
- **Plenum session with invited talks on MIC experience and best practice recommendations**
  (joint session with the Scientific Workshop "High Performance Computing for Water Related Hazards"), public session

- 13:00-13:45 Andrey Semin, Intel: "Intel Xeon Phi (Knights Landing) optimisation best known methods"
- 13:45-14:30 Jan Eitzinger, RRZE: "Evaluation of Intel Xeon Phi "Knights Corner": Opportunities and Shortcomings"
- **14:30-14:45 Coffee Break**
- 14:45-15:30 Serhiy Mochalskyy, IPP: "Simulation using MIC co-processor on HELIOS"
- 15:30-16:15 Vit Vondrak, IT4Innovations: "ESPRESO solver based on hybrid FETI method on MIC architecture"
- **16:15-16:30 Coffee Break**
- 16:30-17:15 Michael Bader, IPCC@TUM: "Experiences with earthquake and tsunami simulation on Xeon Phi platforms"
- 17:15-18:00 Luigi Iapichino / Fabio Baruffa, IPCC@LRZ: "Towards modernisation of the Gadget code on many-core architectures"
Intel Xeon Phi @ LRZ and EU
Evaluating Accelerators at LRZ

Research at LRZ within PRACE & KONWIHR:

● **CELL programming**
  - IBM announced to discontinue CELL in Nov. 2009.

● **GPGPU programming**
  - Regular GPGPU computing courses at LRZ since 2009.
  - Evaluation of GPGPU programming languages:
    - CAPS HMPP
    - PGI accelerator compiler
    - CUDA, cuBLAS, cuFFT
    - PyCUDA/R

● **RapidMind → ArBB (Intel) → discontinued**

● **Knights Ferry (2010) → Knights Corner → Intel Xeon Phi**
New Intel Parallel Computing Centre (IPCC) since July 2014: Extreme Scaling on MIC/x86

Chair of Scientific Computing at the Department of Informatics in the Technische Universität München (TUM) & LRZ

https://software.intel.com/de-de/ipcc#centers


Codes:
- Simulation of Dynamic Ruptures and Seismic Motion in Complex Domains: SeisSol
- Numerical Simulation of Cosmological Structure Formation: GADGET
- Molecular Dynamics Simulation for Chemical Engineering: ls1 mardyn
- Data Mining in High Dimensional Domains Using Sparse Grids: SG++
PRACE: Best Practice Guides

- http://www.prace-ri.eu/best-practice-guides/
- Best Practice Guide – Hydra, March 2013 [PDF HTML]
- Best Practice Guide – JUROPA, March 2013 [PDF HTML]
- Best Practice Guide – Anselm, June 2013 [PDF HTML]
- Best Practice Guide – Curie, November 2013 [PDF HTML]
- Best Practice Guide – Blue Gene/Q, January 2014 [PDF HTML]
- Best Practice Guide – Intel Xeon Phi, February 2014 [PDF HTML]
- Best Practice Guide - JUGENE, June 2012 [PDF HTML]
- Best Practice Guide - Cray XE-XC, December 2013 [PDF HTML]
- Best Practice Guide - IBM Power, June 2012 [PDF HTML]
- Best Practice Guide - IBM Power 775, November 2013 [PDF HTML]
- Best Practice Guide - Chimera, April 2013 [PDF HTML]
- Best Practice Guide - GPGPU, May 2013 [PDF HTML]
- Best Practice Guide - Jade, February 2013 [PDF HTML]
- Best Practice Guide - Stokes, February 2013 [PDF HTML]
- Best Practice Guide - SuperMUC, May 2013 [PDF HTML]
- Best Practice Guide - Generic x86, May 2013 [PDF HTML]

New guides will be published in PRACE-4IP
Intel MIC within PRACE: Best Practice Guide

- Best Practice Guide – Intel Xeon Phi

  - Created within PRACE-3IP.
  - Written in Docbook XML.
  - Michaela Barth (KTH Sweden), Mikko Byckling (CSC Finland), Nevena Ilieva (NCSA Bulgaria), Sami Saarinen (CSC Finland), Michael Schliephake KTH Sweden), Volker Weinberg (LRZ, Editor).
  - http://www.prace-ri.eu/Best-Practice-Guide-Intel-Xeon-Phi-HTML

Update will be done in PRACE-4IP
Applications Enabling for Capability Science

- 27 enabling projects from 17 PRACE partners from 14 countries
  Jul-Dec 2013

- Computations on Eurora (EURopean many integrated cORE Architecture) Prototype at CINECA, Italy with 64 Xeon Phi coprocessors and 64 NVIDIA GPUs


- 16 Whitepapers available online: http://www.prace-project.eu/Evaluation-Intel-MIC
Intel MIC within PRACE: Preparatory Access

- Performance Analysis and Enabling of the RayBen Code for the Intel® MIC Architecture
- Enabling the UCD-SPH code on the Xeon Phi
- Xeon Phi Meets Astrophysical Fluid Dynamics
- Multi-Kepler GPU vs. Multi-Intel MIC for spin systems simulations
- Enabling Smeagol on Xeon Phi: Lessons Learned
- Code Optimization and Scaling of the Astrophysics Software Gadget on Intel Xeon Phi
- Code Optimization and Scalability Testing of an Artificial Bee Colony Based Software for Massively Parallel Multiple Sequence Alignment on the Intel MIC Architecture
- Optimization and Scaling of Multiple Sequence Alignment Software ClustalW on Intel Xeon Phi
- Porting FEASTFLOW to the Intel Xeon Phi: Lessons Learned
- Optimising CP2K for the Intel Xeon Phi
- Towards Porting a Real-World Seismological Application to the Intel MIC Architecture
- FMPS on MIC
- Massively parallel Poisson Equation Solver for hybrid Intel Xeon – Xeon Phi HPC Systems
- Exploiting Locality in Sparse Matrix-Matrix Multiplication on the Many Integrated Core Architecture
- Porting and Verification of ExaFMM Library in MIC Architecture
- AGBNP2 Implicit Solvent Library for Intel® MIC Architecture
Towards Exascale: DEEP & DEEP-ER
Design of an architecture leading to exascale.

Development of hardware:
- Implementation of a Booster based on MIC processors and EXTOLL interconnect.

Energy-aware integration of components:
- Hot-water cooling.

Cluster management system.

Programming environment, programming models.

Libraries and performance analysis tools.

Porting applications.
DEEP Cluster-Booster Architecture
Xeon Phi References

- Books:
    http://lotsofcores.com ; new KNL edition in July 2016!
  - *Parallel Programming and Optimization with Intel Xeon Phi Coprocessors*, Colfax 2013
- Intel Xeon Phi Programming, Training material, CAPS
- Intel Training Material and Webinars
- V. Weinberg (Editor) et al., *Best Practice Guide - Intel Xeon Phi*,
  http://www.prace-project.eu/Best-Practice-Guide-Intel-Xeon-Phi-HTML and references therein
SuperMIC ∈ SuperMUC @ LRZ
SuperMUC System Overview

18x
Island Infiniband switches

non-blocking
SB-EP
16 cores/node
2 GB/core
Compute nodes
18 Thin node islands
(each with 8192 cores)

non-blocking
WM-EX
40 cores/node
6.4 GB/core
Compute nodes
1 Fat node island
(8200 cores)
also used as Migration System

GPFS for $WORK
$SCRATCH

10 PB
... 200 GBs
Parallel Storage

IO nodes
Login Support nodes

Archve and Backup
= 30 PB

Disaster Recovery Site

Peak: 3.26 PF
expected: <3 MW
>155,656 cores

$HOME
1.5 PB / 10 GB/s

NAS
80 Gbit/s

Internet

pruned tree (4:1)

10GBe access
SuperMUC Phase 2: Moving to Haswell

6 Haswell islands
512 nodes per island
warm water cooling

Haswell-EP
24 cores/node
2.67 GB/core

Mellanox FDR14
Island switch
non-blocking

Pruned tree
Spine Infiniband switches

GPFS for
$WORK
$SCRATCH

Parallel Storage
I/O Servers
Login nodes
Support nodes

Thin + Fat islands of SuperMUC

Non-blocking

Mellanox FDR10
Island switch

I/O Servers
(weak coupling of phases 1+2)

LRZ infrastructure
(NAS, Archive, Visualization)
Internet / Grid Services

27-29 June 2016
Intel MIC Programming Workshop
SuperMUC Phase 2: Moving to Haswell
SuperMIC: Intel Xeon Phi Cluster
SuperMIC: Prototype Intel Phi (KNC) System

SuperMUC FDR Infiniband switches (2nd level)  Melanox FDR Infiniband switches  32 Ivy Bridge Nodes with 64 Knight's Corner Many-core accelerators (4352 Cores) Management and login node

10 GE Gateway (NAS, Network)

Dual rail connection
SuperMIC ∈ SuperMUC @ LRZ

- 32 compute nodes (diskless)
  - SLES11 SP3
  - 2 Ivy-Bridge host processors E5-2650@2.6 GHz with 16 cores
  - 2 Intel Xeon Phi 5110P coprocessors per node with 60 cores
  - 64 GB (Host) + 2 * 8 GB (Xeon Phi) memory
  - 2 MLNX CX3 FDR PCIe cards attached to each CPU socket

- Interconnect
  - Mellanox Infiniband FDR14
  - Through Bridge Interface all nodes and MICs are directly accessible

- 1 Login- and 1 Management-Server (Batch-System, xCAT, …)
- Air-cooled
- Supports both native and offload mode
- Batch-system: LoadLeveler
Intel Xeon Phi @ top500 June 2016

- [http://www.top500.org/list/2016/06/](http://www.top500.org/list/2016/06/)
- **#12** Texas Advanced Computing Center/Univ. of Texas United States **Stampede** - PowerEdge C8220, Xeon E5-2680 8C 2.700GHz, Infiniband FDR, Intel Xeon Phi SE10P, Dell
- **#25** (US) / **#34** (USA) / **#42** (China)
- **#55** IT4Innovations National Supercomputing Center, VSB-Technical University of Ostrava Czech Republic **Salomon** - SGI ICE X, Xeon E5-2680v3 12C 2.5GHz, Infiniband FDR, Intel Xeon Phi 7120P, SGI
- **#64** (USA) / **#65** (USA) / **#88** (Japan) / **#100** (USA)
Intel Knights Landing

- June 20, 2016
- Intel Launches ‘Knights Landing’ Phi Family for HPC & Machine Learning

- From ISC 2016 in Frankfurt, Germany, last week, Intel Corp. launched the second-generation Xeon Phi product family, formerly code-named Knights Landing, aimed at HPC and machine learning workloads.
- Will be covered on Wednesday!
And now …

Enjoy the course!
Final remarks
Please fill out the PRACE PATC evaluation form:

https://events.prace-ri.eu/event/494/evaluation/
https://goo.gl/D3Caur

Also linked on Workshop page.

Thank you!
LRZ is part of the Gauss Centre for Supercomputing (GCS), which is one of the six PRACE Advanced Training Centres (PATCs) that started in 2012.

Information on further HPC courses:

- **by LRZ:**
  [http://www.lrz.de/services/compute/courses/](http://www.lrz.de/services/compute/courses/)

- **by the Gauss Centre of Supercomputing (GCS):**
  [http://www.gauss-centre.eu/training](http://www.gauss-centre.eu/training)

- **by the PRACE Advanced Training Centres (PATCs):**
  [http://www.training.prace-ri.eu/](http://www.training.prace-ri.eu/)
Thank you for your participation!